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Inventor: Duane L. Abbey
For: Tailored Response Cascaded Integrator Comb Digital Filter
And Methodology For Parallel Integrator Processing
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Enclosed are:

16 Sheet of Drawings.
 An Assignment of Invention to Rockwell Collins, Inc., Cedar Rapids, IA 52498.
 Combined Declaration and Power of Attorney.
 Information Disclosure Statement and references.

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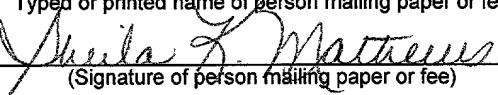
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TAILORED RESPONSE CASCADED INTEGRATOR
COMB DIGITAL FILTER AND METHODOLOGY FOR
PARALLEL INTEGRATOR PROCESSING

By

DUANE L. ABBEY

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FIELD OF THE INVENTION

The present invention generally relates to improved cascaded integrator comb digital filters and more particularly relates to a tailored response cascaded integrator comb filter as a component of an analog-to-digital converter, and even more particularly relates to a pre-decimated cascaded integrator structure and to a tailored response cascaded integrator comb digital filter having an enhanced dynamic range without requiring a higher sample rate.

BACKGROUND OF THE INVENTION

Standard cascaded integrator comb digital filters are well known in the art. They may be used to perform an interpolation function. Interpolation acts to increase an inputted sample rate. In addition, when the positions of the cascaded integrator and cascaded comb sections have been exchanged, they can provide a decimation function. Decimation accomplishes a reduction of an inputted sample rate.

A decimation function is accomplished in such filters by first processing a received signal with a cascade of integrator stages. Following the last integrator stage, the rate is decimated or reduced by a rate change component. For example, if the rate is to be reduced to one-twentieth of the initial rate, the rate change component will accomplish the reduction by dropping nineteen consecutive samples and outputting each twentieth sample. A cascade of comb stages at the lowered rate then processes the samples output by the rate change component.

Cascaded integrator comb digital decimation filters are becoming widely used to reduce the sample rate of highly over-sampled, numerically represented analog signals. Such filters reduce the sample rate and suppress aliased signal folding interference. In addition, they can be configured to recover resolution sufficient to maintain the desired signal to noise ratio.

Unfortunately, the cascaded integrator comb digital decimation filter has a limited dynamic range when the over-sampling ratio is too low. An additional problem results from the fact that the integrator stages must operate at the higher, pre-decimated rate. This imposes a practical limitation on the data rate that can be input to the cascaded integrator stages. Further, such a structure requires higher speed, higher power and therefore more expensive components.

Various types of cascaded integrator comb digital filters have been disclosed in the art. Among these is a parallel cascaded integrator comb filter that is disclosed in U.S. Patent No. 5,596,609 to Genrich et al. This filter, however, has an architecture that is fundamentally different from that of the present invention. The Genrich et al. architecture, for example, generates all possible decimated outputs in each stage of the integrator cascade. In addition, the hardware requirements of the Genrich et al. structure are significantly greater.

Consequently, there exists a need for an improved cascaded integrator comb digital filter having improved bandwidth control without requiring higher sample rates. Further, there exists a need for an improved cascaded integrator structure that reduces the input rate prior to processing by the integrator stages.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an improved cascaded integrator comb digital filter.

It is a feature of the present invention to utilize one or more resonators and multiple rate change components.

It is an advantage of the present invention to achieve greater bandwidth without requiring higher sample rates.

It is another feature of the present invention to perform an alias free rate change prior to initiating processing by the digital filter.

It is another advantage of the present invention to achieve the results of a cascaded integrator comb digital filter using lower power, lower speed and lower cost components.

The present invention includes an apparatus and method for providing an improved cascaded integrator comb digital filter which is designed to satisfy the aforementioned needs, provide the previously stated objects, include the above-listed features and achieve the already articulated advantages. The present invention can be carried out in a cost efficient and "excess-less" manner in the sense that high-speed filter components, capable of handling very high sampling rates, are not required.

Accordingly, the present invention includes a cascaded integrator comb digital filter providing a broader alias protected bandwidth and, in another embodiment, a pre-decimated cascaded integrator structure for a digital filter that is capable of handling faster sampling rates while utilizing lower speed components.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more fully understood by reading the following descriptions of the embodiments of the invention, in conjunction with the appended drawings wherein:

Figure 1 is a block diagram of one embodiment of the general structure of a cascaded integrator comb digital decimation filter.

Figure 2 is a more detailed view of one of the integrator stages of the decimation filter depicted in Figure 1.

Figure 3 is a more detailed view of one of the comb stages of the decimation filter depicted in Figure 1.

Figure 4 is a graphical representation of the performance of the decimation filter depicted in Figure 1, with a 1GS per second input rate.

Figure 5 is a magnified view of a portion of the graphical representation of Figure 4.

Figure 6 is a graphical representation of the phase performance of the decimation filter depicted in Figure 1.

Figure 7 is a block diagram of one embodiment of a tailored response cascaded integrator comb decimation filter incorporating the teachings of the present invention.

Figure 8 is a more detailed view of a resonator stage capable of being used in the tailored response cascaded integrator comb digital decimation filter depicted in Figure 7.

Figure 9 is a block diagram depicting a tailored response cascaded integrator comb digital filter coupled with a signal over-sampling component.

Figure 10 is a graphical representation of the performance of the tailored response cascaded integrator comb digital filter depicted in Figure 7, with a 1GS per second input rate.

Figure 11 is a magnified view of a portion of the graphical representation of Figure 10.

Figure 12 is a graphical representation of the phase performance of the tailored response cascaded integrator comb digital filter depicted in Figure 7.

Figure 13 is a block diagram of the general structure of the post-decimate by four integrator cascade of Figure 7.

Figure 14 is a block diagram of a pre-decimate by four, four integrator cascade structure in accord with the teachings of the present invention.

Figure 15 is a table depicting the output sequence of various integrator structures having different numbers of integrator stages.

Figure 22 is a set of tables depicting the output sequence of a four stage pre-decimate by four integrator structure, such as the pre-decimate integrator structure of Figure 14 and Figure 20.

Figure 16 depicts an algorithm for determining an entry for an integrator output sequence table, such as the sequence table depicted in Figure 15, as a function of two already determined table entries.

Figure 17 is a table depicting the sequence of coefficients of the "A" terms listed in Figure 15, as extended using the method of Figure 16.

Figure 18 is a set of tables, relating to the four pre-decimate by four signal processing paths and the four integration stages of Figure 14, as well as containing the 4 stage "A" term coefficients of Figure 17 distributed as stage 4 path coefficients.

Figure 19 depicts an algorithm for determining stage 1, stage 2 and stage 3 entries for any of the tables depicted in Figure 18 as a function of two already determined table entries.

Figure 20 is a block diagram of a pre-decimate by four, four integrator cascade structure, in accord with the teachings of the present invention, utilizing coefficients of the stage 1 lines of the tables of Figure 18 as the multipliers.

Figure 21 is a table depicting the output sequence of a four stage post-decimate by four integrator structure, such as the post-decimate integrator structure of Figure 13.

DETAILED DESCRIPTION

Now referring to the drawings, wherein like numerals refer to like matter throughout, there is shown in Figure 1 an embodiment of a standard cascaded integrator comb (CIC) digital filter. Cascaded integrator comb filters may be configured to provide either an interpolation or a decimation function. The filter 100 depicted in Figure 1 is a CIC digital decimation filter. Decimation filter 100 is a four stage filter having four integrator stages 102, 104, 106, 108 in a cascaded, or serial, orientation. Data output from the fourth integrator stage 108 is decimated by a factor of twenty by a rate change component 110.

In operation, data is input 112 to the first integrator stage 102 at a given rate, for example, a 1GS per second input rate. When data is output by the fourth integrator stage 108, nineteen of every twenty samples are dropped by rate change component 110. This effectively reduces the input rate of 1GS/s to a rate of 50MS/s upon being output 113 from the rate change component 110. In more general terms, data input to the first integrator stage 102 at a rate of f_s is output 113 from the rate change component 110 at a rate of f_s/R , where R represents the rate change factor. The rate change factor of twenty in Figure 1 is merely an example of one possible rate change factor. Other rate change factors are also used in standard CIC digital filters.

After the rate change, the data is processed by four cascaded comb stages 114, 116, 118, 120. Each of the comb stages has a differential delay of

one sample ($M = 1$). Other delay values may be used however, but generally no more than $M = 2$ due to dilution of performance. Although not required, both integrator and comb stages may be implemented with a series delay for pipelining the signal flow from stage to stage.

The number of integrator and comb stages depicted in Figure 1 is representative of only one embodiment of a CIC digital filter. It is required, however, that the number of comb and integrator stages be equal. Figure 1, for example, shows four integrator 102, 104, 106, 108 and four comb stages 114, 116, 118, 120. Alternatively, other CIC filters may have one, two, three, five or some other number (N) of stages.

Figure 2 is a typical depiction of an integrator stage 200 such as those depicted by the four integrator stages 102, 104, 106, 108 of Figure 1. The system function for an integrator stage 200 such as that depicted in Figure 2 may be represented as $z^1/(1 - z^1)$. Likewise, Figure 3 depicts a comb stage 300 such as those depicted by the four comb stages 114, 116, 118, 120 of Figure 1. The system function for a comb stage 300 such as that depicted in Figure 3 may be represented as $z^1 - z^{(M+1)}$.

The standard CIC filter is described in detail by Hogenauer, E.B. in "An Economical Class of Digital Filters for Decimation and Interpolation": IEEE Transactions on Acoustics, Speech and Signal Processing, Vol. ASSP-29, No. 2,

April 1981, pp. 155-162, which is hereby incorporated herein by reference in its entirety including all figures and appendices.

Figure 4 depicts a power spectral plot of the typical performance of the standard CIC digital filter depicted in Figure 1. The input sample rate is 1GS per second, so the plot is representative of the filter response before decimation and spectral folding. The four comb stages 114, 116, 118, 120 of Figure 1 place four zeros at each increment (50MHz, 100MHz, 150MHz, 200MHz, etc.) of the reduced output rate (f_s/R) resulting in several notches 402, 404, 406, 408, 410, 412. The roll off of the several side lobe responses 414, 416, 418, 420, 422 is generated by the four integrator stages 102, 104, 106, 108 of Figure 1.

Figure 5 depicts an enlarged view of the main lobe response 500 of Fig. 5, 424 of Fig. 4. Figure 5 also depicts the folded noise response 502 after the decimation to 50MHz. It is noted, for example, that at a signal to noise ratio of 80dB, there is provided 4.25MHz of real bandwidth 504. A complex pair of filters would provide +/-4.25MHz of complex bandwidth. Figure 6 illustrates that the filter of Figure 1 is a linear phase filter exhibiting minimal distortion in the signal bandwidth.

Figure 7 depicts an embodiment of a tailored response CIC digital filter 700 of the present invention. The tailored response CIC digital filter 700 is an embodiment of a four stage decimation filter having four integrator stages 702, 704, 706, 708 in a cascaded orientation. Data output from the fourth integrator

stage 708 is decimated by a factor of four by a rate change component 710.

Data is then passed 712 from the rate change component 710 to a comb stage 714 at the first reduced rate.

For example, for a 1GS/s input rate 716 (f_s), the output 712 from the rate change component 710 has a rate of 250MS/s (f_s/R_1). The first rate change factor of four in Figure 7 is merely an example of one possible rate change factor. Other rate change factors may also be used. For example, other embodiments of the present invention have different numbers of stages, different rate change factors, and possibly different numbers of rate change elements, all in appropriate combination for the desired level of performance.

Data output from the rate change component 710 is processed by three cascaded comb stages 714, 718, 720. The notch width (see 1002, 1004, 1006 or 1008 of Fig. 10) at multiples of the lowered rate can be broadened by tailoring the delay length (M) at the higher sample rates. The broadened notches result in a wider alias-protected bandwidth following final decimation by a second rate change component 722.

In the embodiment of Figure 7, each of the comb stages has a different delay length. The first comb stage 714 has a differential delay of six samples ($M = 6$). The second 718 and third 720 comb stages have differential delays of seven ($M = 7$) and eight ($M = 8$) samples respectively. In other embodiments, other delay values may be used.

Data output by the third comb stage 720 is input to 726 and processed by a resonator stage 724. One type of resonator suitable for use with the present invention is the corner resonator stage 800 depicted in Figure 8. It will be appreciated that other types of resonators and/or multiple resonators can be used in other embodiments of the present invention. Data output 728 from the resonator 724 of Fig. 7, 800 of Fig. 8, is input to the second rate change component 722.

Referring to the resonator 724 of Fig. 7, 800 of Fig. 8, the "T" value 802 of the resonator is set such that the low pass resonance corner frequency flattens and widens the pass band (see 1010, Fig. 10) of the main response lobe 1012, Fig. 10. The "G" value 804 of the resonator 724 of Fig. 7, 800 of Fig. 8, is set to control the amplitude of the resonator output at the main lobe corner frequency.

Data received by the second rate change component 722 is decimated by a factor of five and is passed at the second reduced rate to a fourth comb stage 730. For example, for the 250MS/s reduced rate output 712 from the first rate change component 710 (f_s/R_1), the output 732 from the second rate change component 722 has a second reduced rate of 50MS/s ($(f_s/R_1)/R_2$). As with the first rate change factor (R_1) of four, the second rate change factor (R_2) of Figure 7 is also merely an example of one possible rate change factor. Other rate change factors may also be used.

The fourth comb stage 730 has a differential delay of one sample ($M = 1$).

The fourth comb stage 730 also adds its contribution to each of the notches 1002, 1004, 1006 or 1008 of Fig. 10 positioned at integer multiples (50MHz, 100MHz, 150MHz, etc.) of the second reduced rate. Finally, the fourth comb stage 730 outputs its data 734 to the next component of the system at the second reduced rate.

Figure 9 depicts the general relationship of the tailored response CIC digital filter of the present invention to other cooperating components. In Figure 9, a signal 900 is received and is processed by a signal over-sampling component 902. The signal over-sampling component 902 can be virtually any component providing an over-sampling of a signal 900. For example, in one embodiment the signal over-sampling component 902 can be a delta-sigma modulator sampling a signal 900 at a rate of f_s .

The signal over-sampling component 902 outputs 904 an "n" bit data element to the tailored response CIC digital filter 906. The "n" bit data element will typically be a one bit element, but other embodiments may pass an element having a greater number of bits. The tailored response CIC digital filter 906 receives the data element at the input rate of f_s . After processing, the tailored response CIC digital filter 906 outputs 908 an "m" bit data element at the reduced rate of f_s/R . The number of bits output 908 by the tailored response CIC digital filter 906 is determined as a function of the in-band noise suppression desired and/or available after decimation.

The tailored response CIC digital filter 906 can be the decimation filter disclosed above in relation to Figures 7 and 8. The structure of Figure 9 would be particularly useful, for example, in a delta-sigma modulator type analog to digital converter. The present invention permits use of lower speed, lower power and lower cost components for the filter than would otherwise be possible. Further, the present invention facilitates development of high dynamic range/wide bandwidth analog to digital converters. It will also facilitate development of a direct sampling communications receiver.

Figure 10 depicts a power spectral plot of the typical performance of the tailored response CIC digital filter depicted in Figure 7. The input sample rate is 1GS per second, so the plot is representative of the filter response before decimation and spectral folding. The four comb stages 714, 718, 720, 730 of Figure 7 place zeros at different frequencies (and multiples thereof) determined by $f_s/(R^*M)$. Multiples of 31.25MHz, 35.7MHz, 41.7MHz and 50MHz are produced for $M = 8, 7, 6$ and 1 respectively. The resulting several notches 1002, 1004, 1006, 1008 are formed from composites of the notch multiple groupings. The faster response roll off of the several side lobe responses 1014, 1016, 1018, 1020 and the wider bandwidth of the main lobe response 1012 is apparent in Figure 10.

Figure 11 depicts an enlarged view of the main lobe response 1100 of Fig. 11, 1012 of Fig. 10. Note that the null depth resolution is greater in Figure 11 than in Figure 10, but is still limited by the simulation's numeric accuracy. Figure

11 also depicts the folded noise response 1102 after the decimation to 50MHz. At a signal to noise ratio of 80dB, there is now provided 16.3MHz of real bandwidth 1104. A complex pair of filters would provide +/-16.3MHz of complex bandwidth. This is nearly four times wider than the 4.25MHz of bandwidth 504 depicted in Figure 5 in relation to the standard CIC digital filter. Figure 12 illustrates that, through the signal and transition bandwidths, the filter of Figure 7 is a linear phase filter exhibiting minimal distortion in the signal bandwidth. The tailored comb stages produce phase jumps in the stop bandwidths, but with no amplitude to corrupt the signal bandwidth after the final decimation.

The tailored response CIC digital decimation filter of the present invention can have any number of integrator and comb stages on a one-for-one basis. By running part or all of the comb stages at a higher sample rate than the output rate, and by using appropriate delay values for each stage, fractional delay values are effectively established at the filter output sample rate. For example, in the embodiment of Figure 7, with respect to the second rate change factor of five, the delay values of the first 714, second 718 and third 720 comb stages ($M = 6$, $M = 7$, $M = 8$, respectively) equate to values of $6/5$, $7/5$ and $8/5$ at the 50MS/s output sample rate. These notch placements, and the final notch placement provided by the fourth comb stage 730 at a value of $5/5$, result in greatly improved noise suppression over wider pass bands.

Further, the present invention can have intermediate sample rate corner resonators as required to shape the band pass and increase the transition band

roll off rate. For example, the tailored response CIC digital decimation filter described in relation to Figure 7 could include zero, one, two or more such resonators, with resonance frequencies placed to optimize pass bandwidth and minimize pass band ripple.

Figure 13 depicts a cascaded integrator section 1300 with a rate change component 1310. The structure of Figure 13 is similar to the integrator structure depicted in Figure 7. The cascaded integrators 1302, 1304, 1306, 1308 correspond to the four integrators 702, 704, 706, 708 of Figure 7 with the integrator structure of Figure 2 substituted for each block depiction of Figure 7. Since the rate change component 1310 performs the decimation after all of the integrator stages have been executed, this structure will be referred to as a post-decimate structure.

Figure 14 depicts a parallel processed, pre-decimate by four, four integrator cascade structure (digital filter section) that is functionally equivalent to the filter section of Figure 13. The filter section of Figure 14, however, is structurally and operationally different from the functionally equivalent filter of Figure 13. In the structure of Figure 14, the decimation or rate change is accomplished prior to processing by any of the integrator stages 1402, 1404, 1406, 1408. When the filter input is demultiplexed (serial to parallel rate reduction by four) as in Figure 14, the input integrations can be performed at a lower sample rate.

The structure of Figure 14 could replace the integrator stages 702, 704, 706, 708 and the rate change component 710 of the tailored response CIC digital filter of Figure 7. Further, structures such as those disclosed in Figure 14, but having a different number of integrator stages or a different rate change factor, could replace integrator and rate change components of other CIC filters having an equivalent number of integrator stages. For example, if the structure of Figure 14 included a rate change factor of twenty instead of four, it could replace the integrator stages 102, 104, 106, 108 and the rate change component 110 of the standard CIC digital filter of Figure 1.

In operation, a serial sampled signal 1410 is input to a serial sample to parallel sample converter 1412. The serial sample to parallel sample converter 1412 and its associated delay register 1414 converts the received serial sample signal 1410 into four delayed parallel signal paths 1416, each path having been decimated by a factor of four. These delayed signal paths, as well as further delayed signal paths, are fed to various multipliers 1418, 1432, 1436, 1440, 1444, 1448, 1452, 1456, 1460 where they are multiplied by the indicated coefficients 1420, 1434, 1438, 1442, 1446, 1450, 1454, 1458, 1462 and summed 1422, 1423 as shown.

The delayed signal paths are also pre-summed 1424. The summation of the pre-summed signals 1424 is input to a multiplier 1426 and multiplied by a coefficient 1428 of sixty-four. The product obtained by the multiplier 1426 is processed by the first integrator stage 1402. The output of the first integrator

stage 1402 is then summed into the prior summation 1423. Finally, the output of the final summation 1423 is passed through the second 1404, third 1406 and fourth 1408 integrator stages. If the structure of Figure 14 was used to replace the integrator stages 702, 704, 706, 708 and the first rate change component 710 of Figure 7, for example, the output 1430 of the fourth integrator stage 1408 would be input to the first comb stage 714 of Figure 7.

Figures 15-20 illustrate a methodology that can be used to develop the parallel integrator processing structure such as that depicted in Figure 14. This methodology can be followed in developing various other embodiments of the present invention. For example, the methodology to be disclosed can be used to develop a parallel integrator processing structure having one through eight or more integrator stages. To illustrate the methodology, Figures 15 through 20 will be used to generate the structure disclosed in Figure 14.

Figure 15 depicts a table that can be used for generating a parallel integrator processing structure having anywhere from one to eight stages. In developing the four integrator stage structure of Figure 14, the row referring to "4 Stages" 1500 is used. The right-hand column of each row lists the output sequence obtained by passing an input sequence of "A, B, C, D, E . . ." through a cascade of the indicated number of integrator stages. For example, if a sequence of "A, B, C, D . . ." were input 112 into the four cascaded integrator stages 102, 104, 106, 108, the output of the fourth integrator stage 108 would be

"0, 0, 0, 0, A, 4A + B, 10A + 4B + C, 20A + 10B + 4C + D, . . ." as indicated in the "4 Stages" row 1500 of Figure 15.

Figure 16 illustrates a method useful for creating and extending the table of Figure 15. The next term in a given sequence can be generated from two earlier calculated terms. For instance, the eleventh term 1502 in the sequence for "8 Stages" can be calculated by adding the tenth term 1504 of the "7 Stages" sequence, $28A + 7B + C$, to the tenth term 1506 of the "8 Stages" sequence, $8A + B$. The table can be extended to "9 Stages" by listing a zero for the initial term and by generating the successive terms via the method of Figure 16. In similar fashion, the table can be extended to include more than nine stages.

Figure 17 depicts a table listing a sequence of the "A" coefficients or multipliers for each term generated in Figure 15. Note that the "B" coefficients can be determined from the "A" coefficients of Figure 15 by using the "A" coefficient of the prior term. In a similar manner, "C," "D," "E," etc., coefficients can be determined from "B," "C," "D," etc., coefficients respectively.

Since a pre-decimate by four integrator structure is being developed with four parallel paths directed into the filter, the coefficients of the "4 Stages" row 1700 of the coefficient table of Figure 17 must also be demultiplexed into four paths. Figure 18 depicts tables for each of the four paths. Leading zeros in each of the rows of Figure 17 are discarded in Figure 18.

Generation of the “Stage 4” rows of Figure 18 will now be illustrated.

Referring to the “4 Stages” row 1700 of Figure 17, the first non-zero “A” coefficient listed is “1.” The sequence must be decimated by four. The next term of the sequence is therefore “35.” Skipping three more terms, the next term is “165.” The terms of this decimated by four sequence appear in the “Stage 4” row 1800 of the “Path 4” table of Figure 18.

Next, the “Stage 4” row 1802 of the “Path 3” table is determined. These terms are also obtained by decimating the “4 Stages” row 1700 of Figure 17 by a factor of four. The “Path 3” sequence, however, is generated by starting with the second non-zero “A” coefficient of the “4 Stages” row 1700. Hence, the “Stage 4” terms for “Path 3” are found to be “4, 56, 220, 560 . . .” The “Stage 4” rows 1804, 1806 of the “Path 2” and “Path 1” tables are similarly generated by beginning with the third and fourth non-zero “A” coefficients respectively of the “4 Stages” row 1700.

Figure 19 illustrates a method for generating the “Stage 3,” “Stage 2” and “Stage 1” rows for the four tables of Figure 18. For example, in the “Path 1” table, the second term of the “Stage 3” row can be generated from the first and second terms of the “Stage 4” row. Following the method of Figure 19, the first term of the “Stage 4” row, “20,” is subtracted from second term of the “Stage 4” row, “120,” to yield the second term of the “Stage 3” row, “100.” To determine the first term of each row, zero is subtracted from the value of the first term of the

row immediately above the term being determined. By following this method, each of the rows of Figure 18 can be generated.

Figure 20 depicts a structure functionally equivalent to the structure of Figure 14. Figure 20 is generated using the terms of the "Stage 1" rows of Figure 18. First, the "Stage 1" row of the "Path 1" table of Figure 18 is included in the structure. In Figure 20, the first coefficient of the row, "20," is applied to the sample of the first path 2000 by a first multiplier 2002. The next coefficient of the row, "60," is applied by a second multiplier 2004 to those samples of the first path 2000 that have been delayed by a factor of one sample. The third coefficient, "64," is a repeating coefficient that is applied, via a third multiplier 2006, to all samples of the first path 2000 that have been delayed by a factor of two or more samples. This recursive delay, multiply by "64," and combine process is accomplished by integrating the output of multiplier 2006 with a first integrator 2012. The outputs of the first integrator 2012 and multipliers 2002, 2004 are then summed 2008. The result of the summation 2008 is processed by a cascade of three additional integrators 2010 to complete the four integrator stages for the first path 2000. In a similar fashion, the remaining "Stage 1" coefficients of Figure 18 are included in the structure of Figure 20, the outputs of which are all summed with the output of integrators 2010 to form the filter section output 1430.

After completing a structure such as depicted in Figure 20, a streamlined structure such as that depicted in Figure 14 is created. Figure 14 is obtained by combining linear processing that is applied to each of the four paths. The

structure of Figure 14 has fewer multipliers, adders and integrators than does the structure of Figure 20. Further, it is noted that, given that the input data samples are typically one bit each, the coefficient multiplies and accumulates can be performed in part by a read only memory using the delayed path data samples as address bits. Use of a read only memory in such a way will reduce the amount of hardware required and will help maintain a high processing speed.

Figures 21 and 22 depict tables used to verify that the pre-decimate by four methodology disclosed in relation to Figures 14 to 20 produces results equivalent to those that would be obtained via the post-decimate by four structure of Figure 13. Figure 21 depicts the sequence of outputs that would be output from the fourth integrator stage 1308 of the post-decimate by four structure of Figure 13 upon receiving “A, B, C, D, E . . .” as input. The underlined terms in Figure 21 indicate the output from the rate change component 1310 after the decimation. In Figure 21, there are four different ways that the sequence can be decimated by four. In Figure 21, decimation is accomplished by dropping three terms and keeping each fourth term.

Figure 22 depicts outputs related to the pre-decimate by four structure of Figures 14-20. The lines designated as “Path 1,” “Path 2,” “Path 3” and Path 4” depict the first four outputs generated by each of the four paths. The “Path Sum” sequence of terms is the summation of the terms generated by each of the four paths. For instance, the first term of the “Path Sum” sequence is the summation of the first terms of each of the four paths. Likewise, the second term of the

"Path Sum" sequence, $120A + 84B + 56C + 35D + 20E + 10F + 4G + H$, is the summation of the second term of each of the four paths. This is the algorithm performed by Figure 20 and its streamlined, functionally-equivalent structure in Figure 14. As is clear from the underlined terms of Figure 21 and the "Path Sum" sequence of Figure 22, the outputs of the pre-decimate and the post-decimate structures are equivalent.

Using the procedure described above, it is also possible to configure circuits similar to Figure 20 to obtain the other three possible decimated output sequences. This is accomplished by starting with the second, third or fourth leading zero terms of the "4 Stages" row of Figure 17 and then decimating by four. Next, tables similar to those of Figure 18 are generated. The circuit structure is then created using the terms of the "Stage 1" rows as coefficients. Any one of the four possible decimated output sequences, however, is all that is generally required.

While the pre-decimate structure has been illustrated and described for an apparatus having four integrator stages and a rate change factor of four, in other embodiments the invention has a different number of stages, a different rate change factor or both. In general, the invention can be said to work for a structure having "n" stages and a rate change factor of "r" (where "n" and "r" are positive integers). The rate change factor "r" determines the number of path tables that would be used, for example, in tables such as the path tables of

Figure 18. The number of stages "n" determines the number of rows that would be included in each Figure 18 type of path table.

In addition, it is thought that the method and apparatus of the present invention will be understood from the appended claims and the description provided throughout this specification. Further, it will be apparent that various changes may be made in the form, construct steps and arrangement of the parts and steps thereof without departing from the spirit and scope of the invention or sacrificing its material advantages. The form herein described is merely a preferred exemplary embodiment thereof.

CLAIMS

I claim:

1. A cascaded integrator comb digital filter, comprising:

a cascaded integrator structure;

a cascaded comb structure;

a first rate change component, located between said cascaded integrator structure and said cascaded comb structure; and

a second rate change component, located with said cascaded comb structure.

2. The cascaded integrator comb digital filter according to Claim 1,

wherein said first rate change component subsamples output received from said cascaded integrator structure and outputs a reduced rate signal to said cascaded comb structure.

3. The cascaded integrator comb digital filter according to Claim 1,

wherein said cascaded integrator structure comprises a plurality of integrator stages.

4. The cascaded integrator comb digital filter according to Claim 1,
further comprising a third rate change component.

5. The cascaded integrator comb digital filter according to Claim 1,
further comprising a plurality of additional rate change components.

6. The cascaded integrator comb digital filter according to Claim 1,
further comprising a signal generating component providing an oversampled
signal as input to said cascaded integrator structure.

7. The cascaded integrator comb digital filter according to Claim 6,
wherein said signal generating component comprises a delta-sigma modulator.

8. The cascaded integrator comb digital filter according to Claim 1,
wherein said cascaded integrator structure comprises a plurality of integrator
stages and wherein said cascaded comb structure comprises a plurality of comb
stages, said plurality of integrator stages and said plurality of comb stages having
an equivalent number of stages.

9. The cascaded integrator comb digital filter according to Claim 8, wherein at least two comb stages of said plurality of comb stages have different delay values.

10. The cascaded integrator comb digital filter according to Claim 1, further comprising a resonator component, and wherein said cascaded comb structure comprises a plurality of comb stages.

11. The cascaded integrator comb digital filter according to Claim 10, wherein said resonator component is located between two comb stages of said plurality of comb stages.

12. The cascaded integrator comb digital filter according to Claim 10, further comprising a plurality of resonators located among said plurality of comb stages.

13. A pre-decimated integrator filter section, comprising:

a data rate change component; and

a first integrator structure comprising at one integrator stage, said first integrator structure receiving data at a rate established by said data rate change component, said first integrator structure modifying data received from said data rate change component;

wherein the pre-decimated integrator filter section outputs data equivalent to data that would be output by a post-decimated integrator filter section having an equal number of integrator stages.

14. The pre-decimated integrator filter section according to Claim 13, further comprising a second integrator structure having one or more integrator stages.

15. The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure comprises an integrator stage and a plurality of multipliers.

16. The pre-decimated integrator filter section according to Claim 13, wherein said data rate change component comprises a serial to parallel converter.

17. The pre-decimated integrator filter section according to Claim 13, further comprising a read only memory device, said read only memory device being used by said first integrator structure to modify data received from said data rate change component.

18. The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure modifies data received from said data rate change component by applying coefficients stored in a look-up table.

19. The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure comprises a plurality of reduced rate parallel signal paths with an integrator stage and a plurality of coefficient multipliers for each path.

20. A method of performing a pre-decimated cascaded integration in a filter section, comprising the steps of:

changing the data rate of data being received by an integrator structure;

performing a first integration procedure on data received at the changed data rate, wherein the first integration procedure includes at least one integrator stage;

executing a second integration procedure on data output by said first integration procedure, wherein the second integration procedure includes at least one additional integrator stage; and

outputting data equivalent to data that would be output by a post-decimated cascaded integrator having an equal number of integrator stages.

21. A method according to Claim 20, wherein said executing step comprises processing received data with a plurality of parallel integrator stages.

22. A method according to Claim 20, wherein said changing step comprises converting a received serial data stream to a parallel signal having a plurality of parallel paths and decimating the received data by a factor equal to the number of parallel paths.

23. The method according to Claim 20, wherein said performing step further comprises modifying the received data by multiplication by determined coefficients.

24. The method according to Claim 20, wherein said performing step comprises a step of accessing a memory device, data held by said memory device being used during said performing step to modify data received from said data rate change component.

25. The method according to Claim 20, wherein said performing step includes a combining procedure further modifying data received at the changed data rate.

26. A tailored response cascaded integrator comb digital filter, comprising:
cascaded integrator means;
cascaded comb means;
first rate change means, located between said cascaded integrator means and said cascaded comb means; and
second rate change means, located with said cascaded comb means.

27. The tailored response cascaded integrator comb digital filter according to Claim 26, further comprising a resonator means.

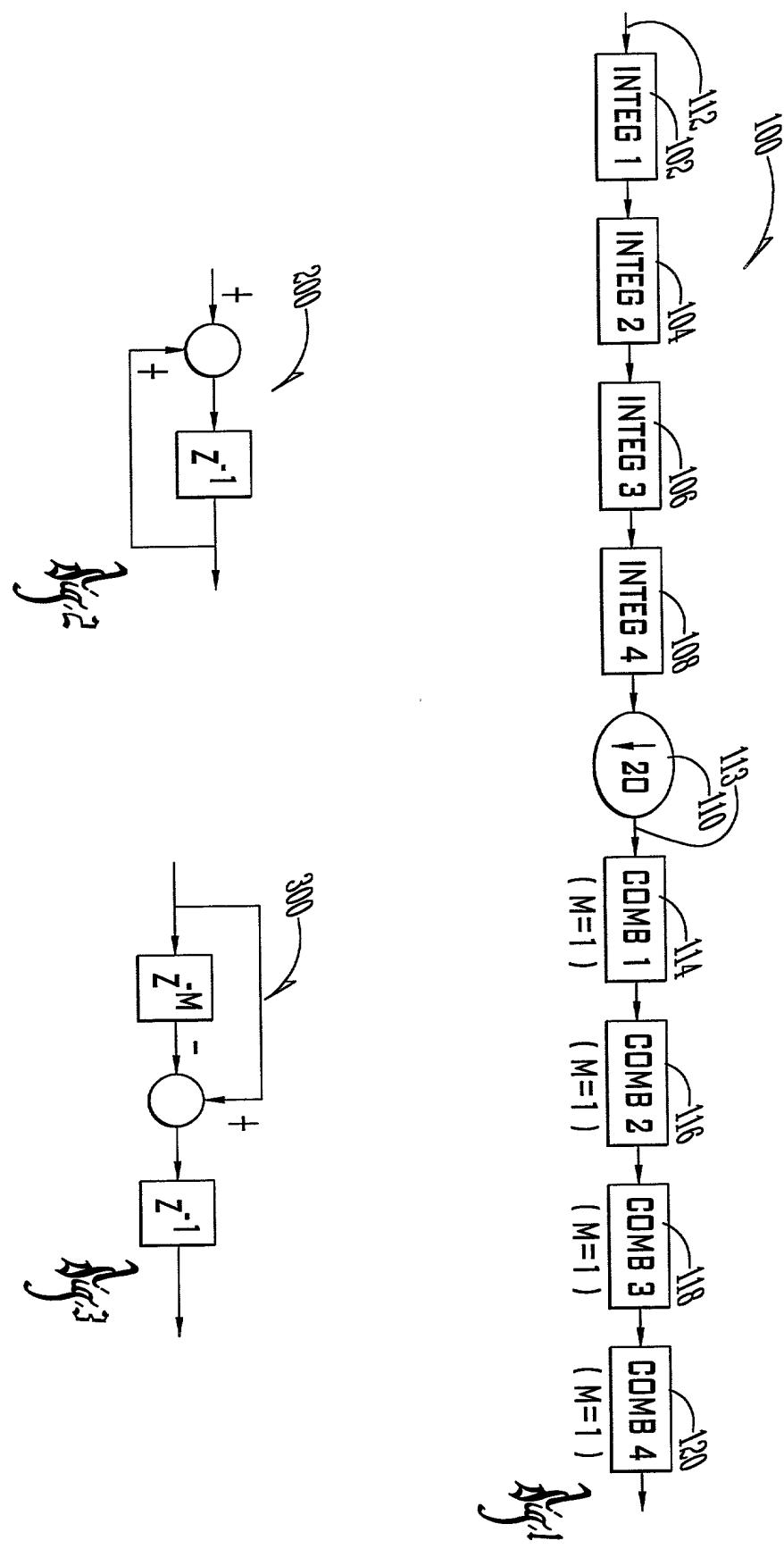
28. The tailored response cascaded integrator comb digital filter according to Claim 27, wherein said resonator means is located with said cascaded comb means.

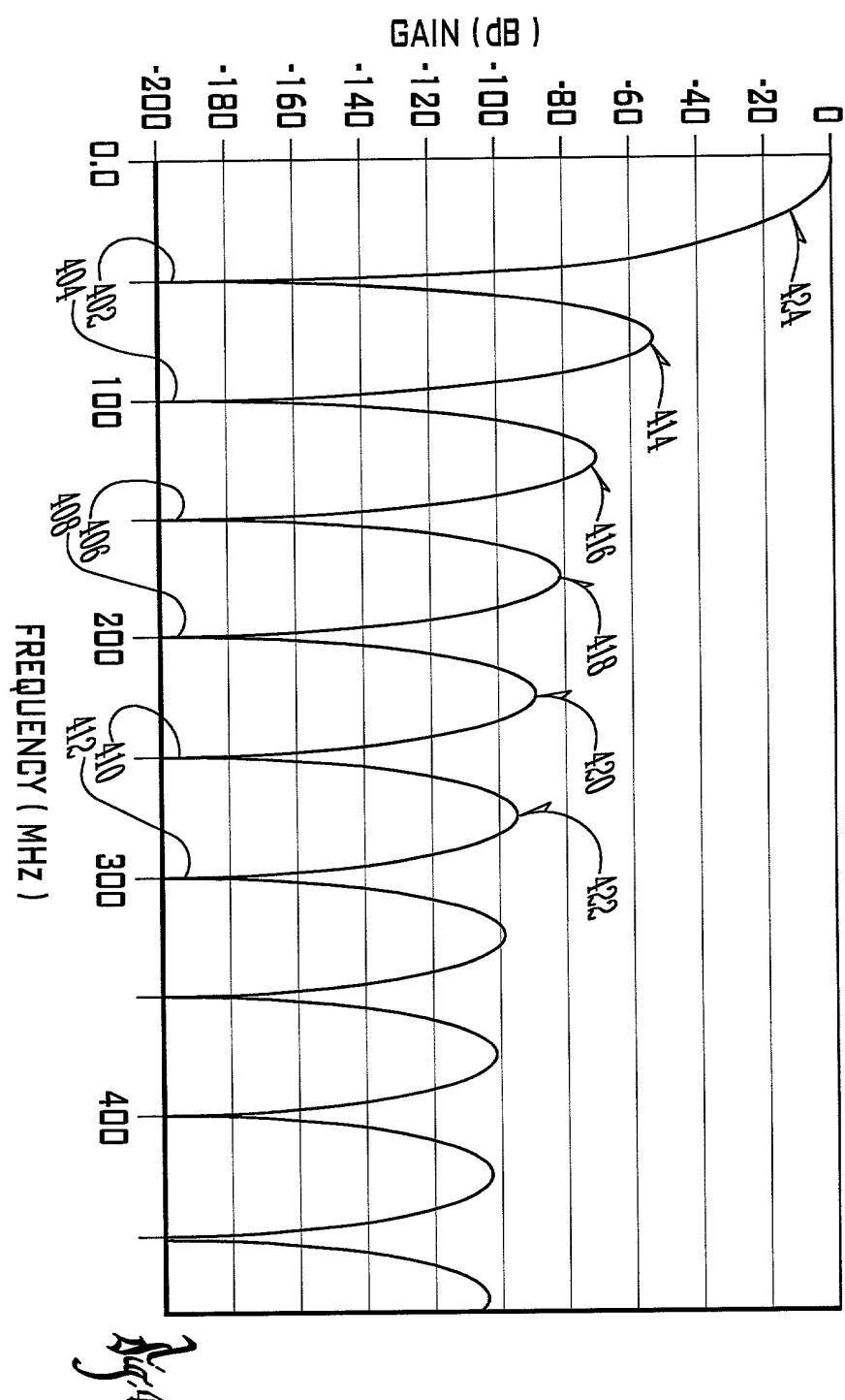
29. The tailored response cascaded integrator comb digital filter according to Claim 26, wherein said cascaded comb means comprises a plurality of comb stages.

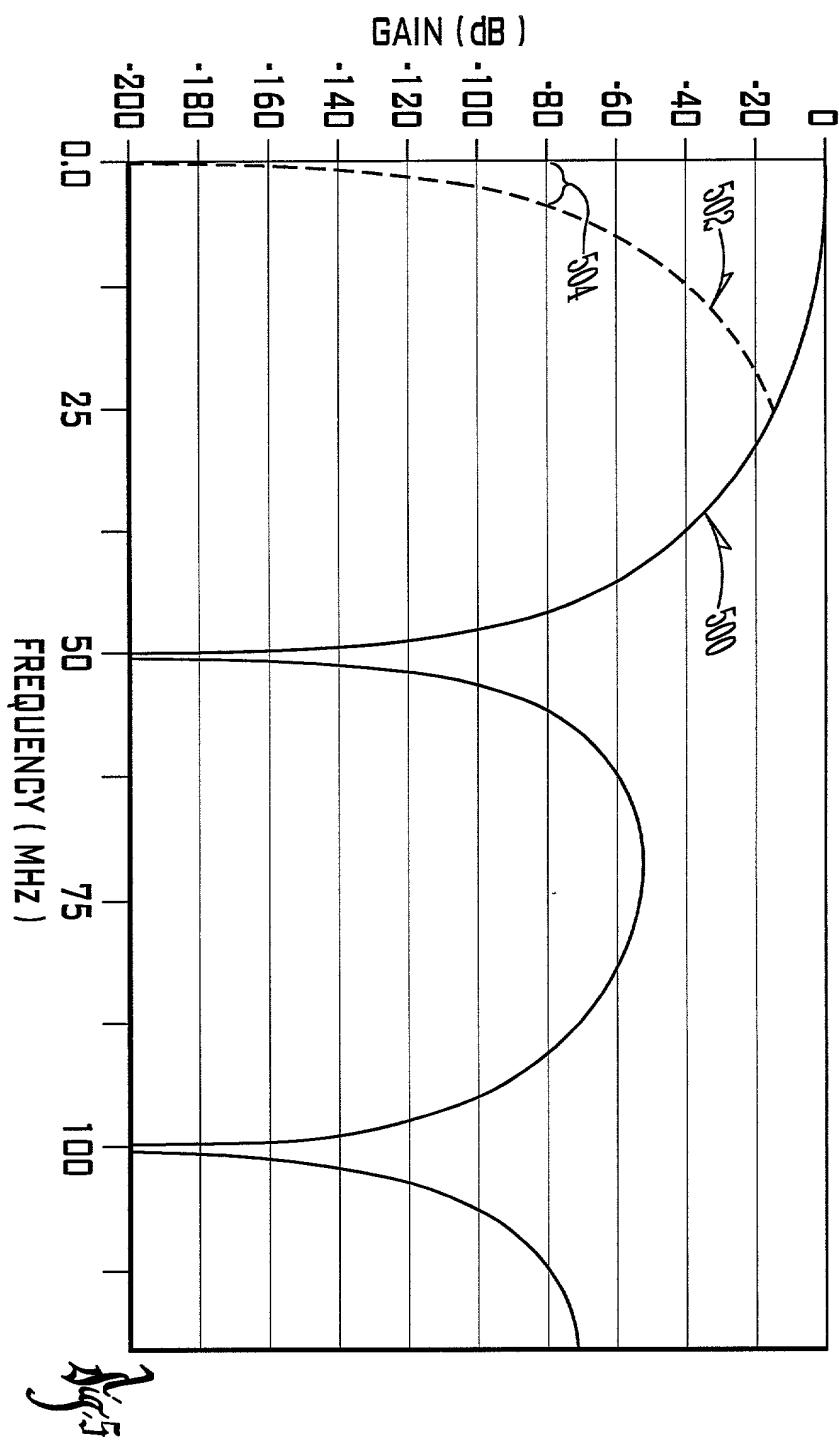
30. The tailored response cascaded integrator comb digital filter according to Claim 29, wherein at least two comb stages of said plurality of comb stages have different delay values.

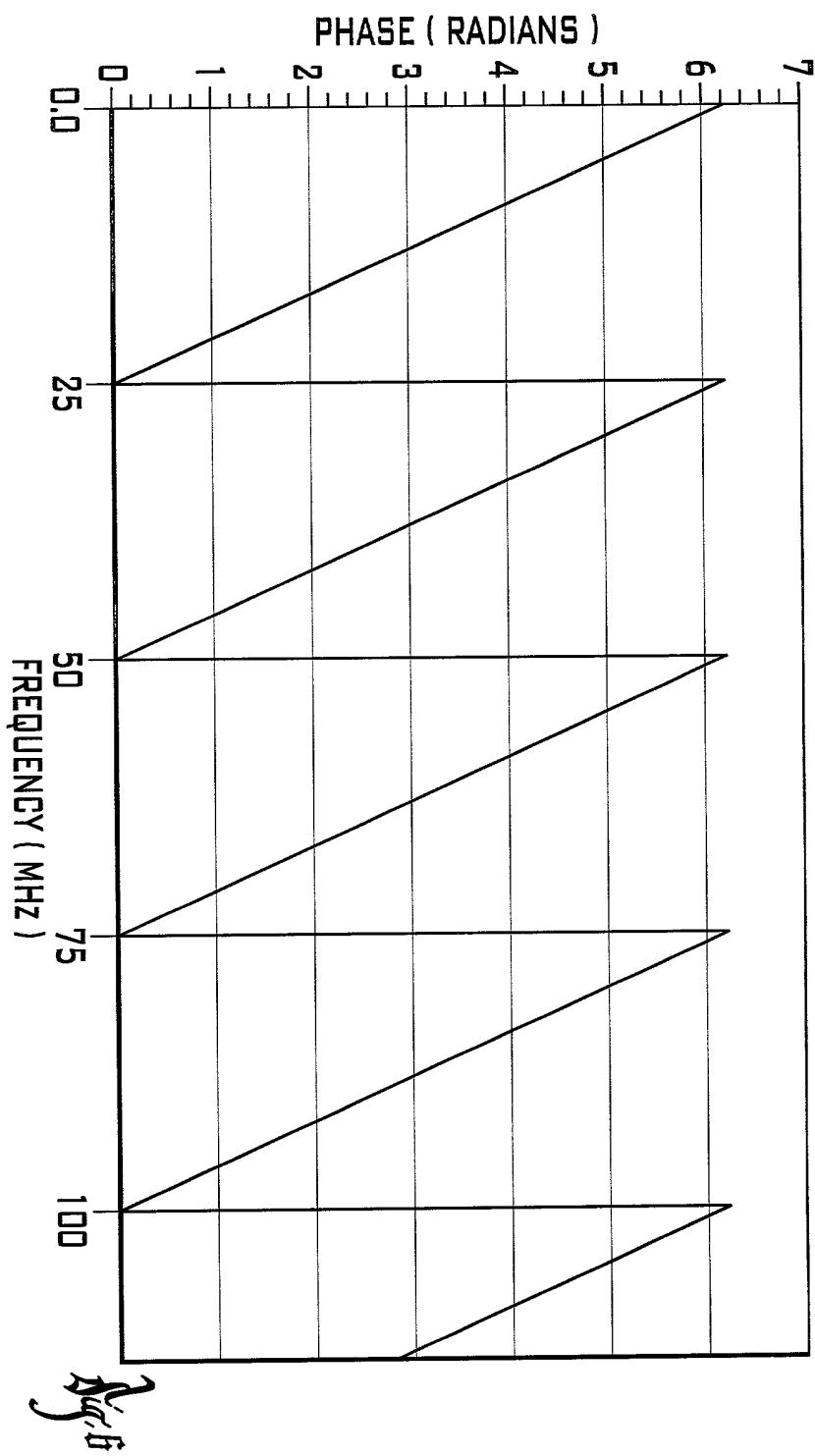
ABSTRACT

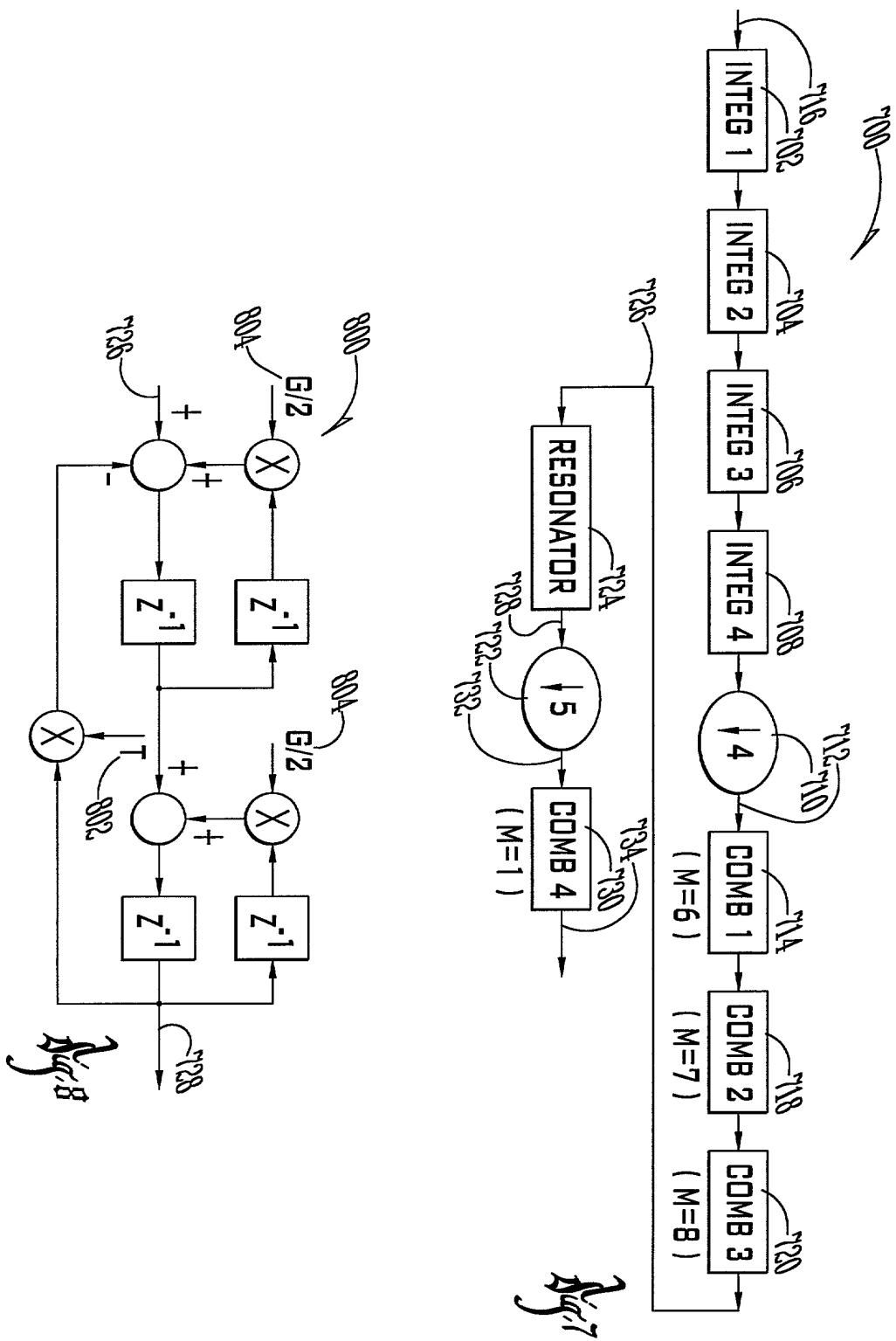
A tailored response cascaded integrator comb digital filter is disclosed which has a cascaded integrator structure, a cascaded comb structure, a first rate change component, a second rate change component and can additionally include a resonator. The improved structure achieves greater bandwidth without requiring higher sampling rates. In an additional embodiment, a pre-decimated cascaded integrator filter section for a cascaded integrator comb digital filter is disclosed as having a data rate change component and a first integrator structure receiving data at the rate established by the data rate change component and modifying the received data. The pre-decimated filter section can also include a second integration structure. The pre-decimate structure outputs data equivalent to data that would be output by a post-decimated cascaded integrator structure having an equal number of cascaded integrator stages.

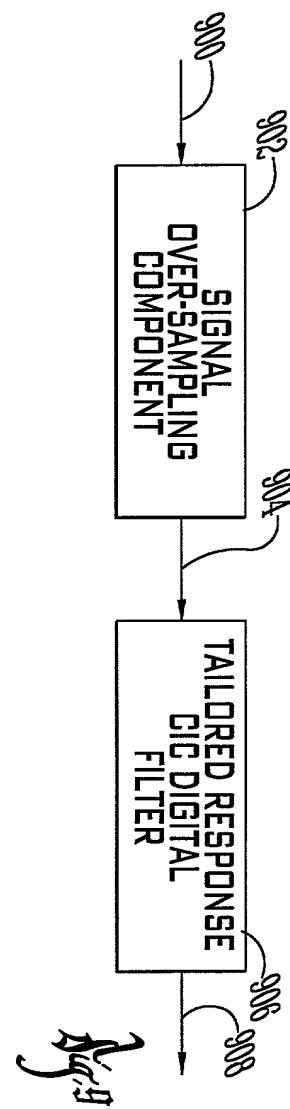


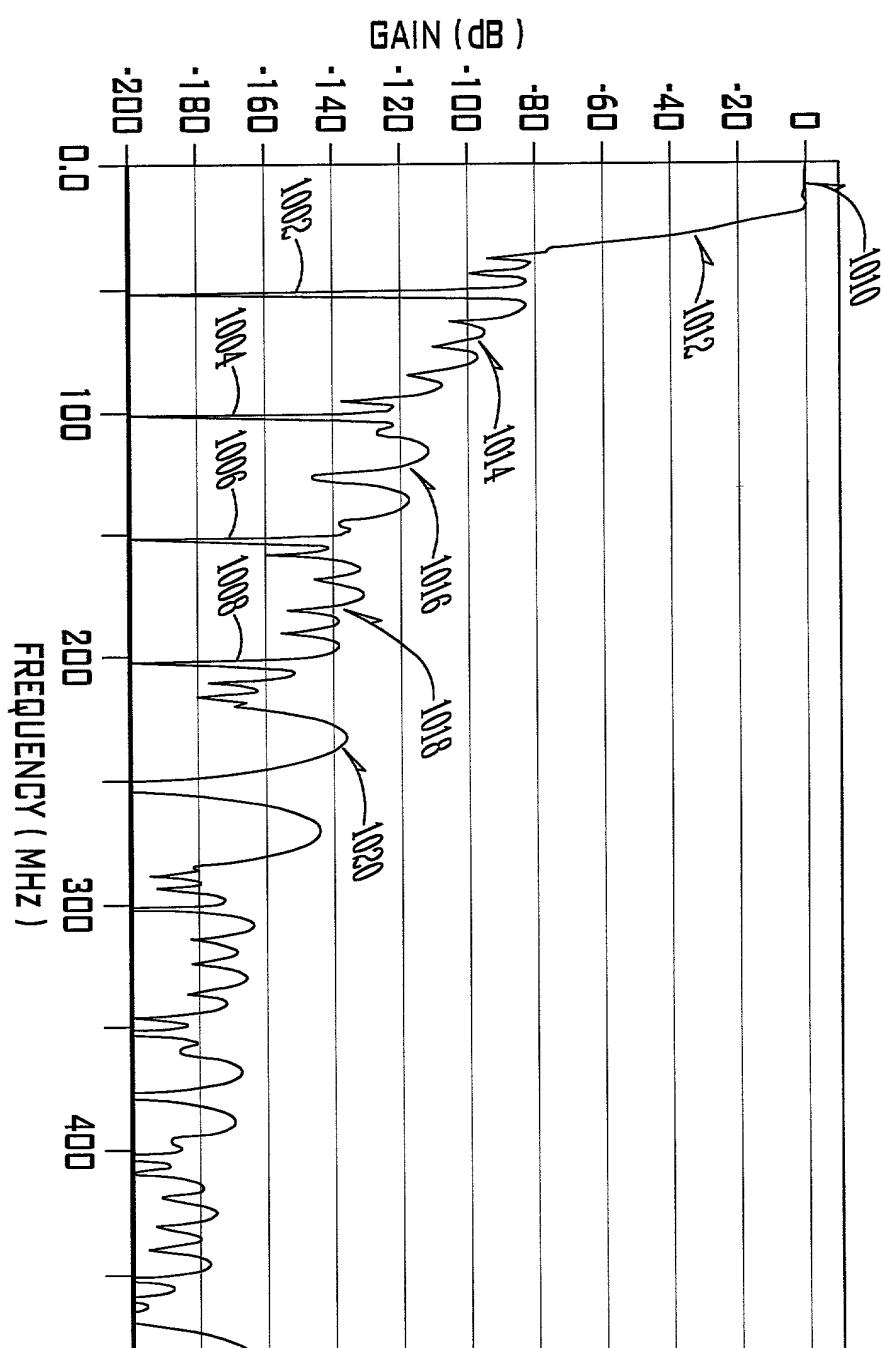


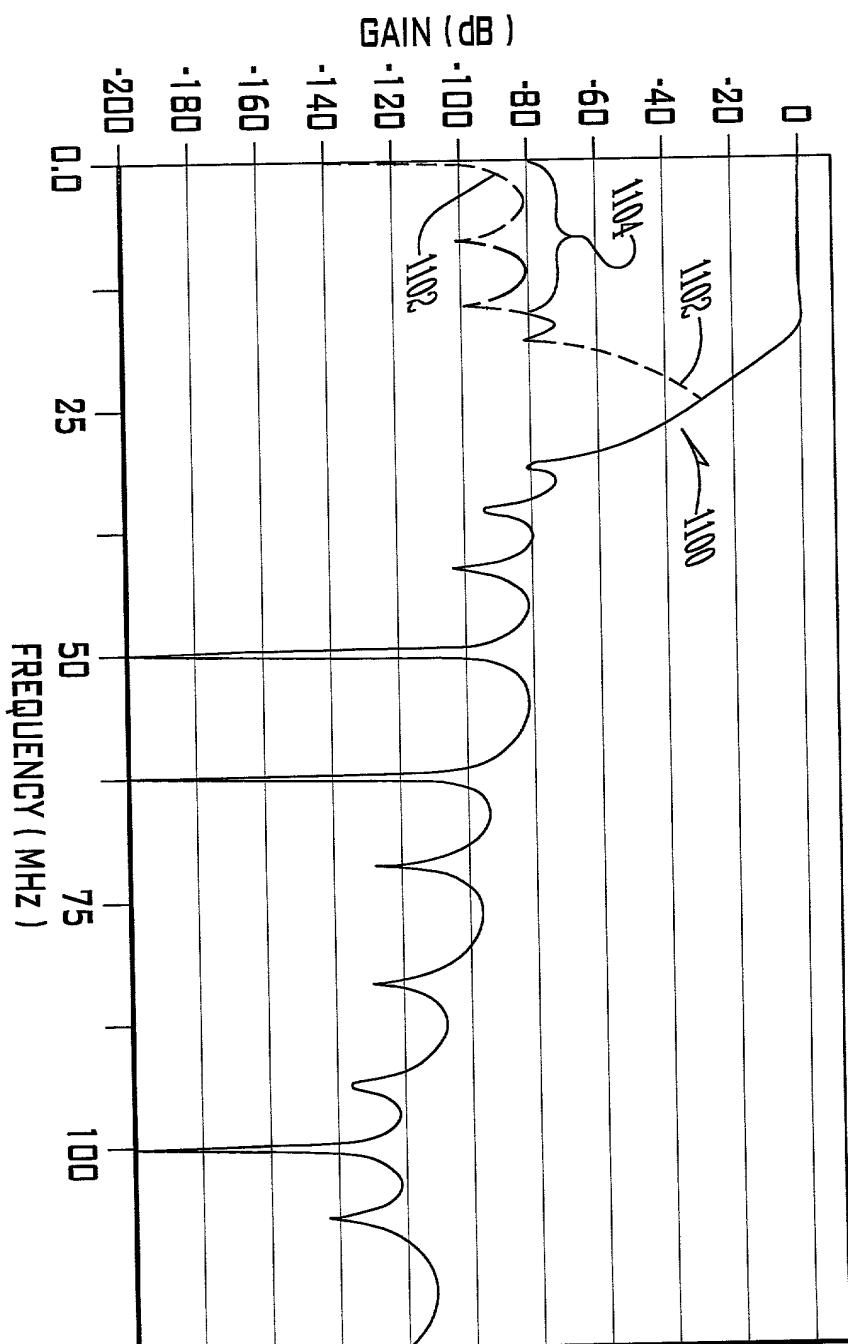




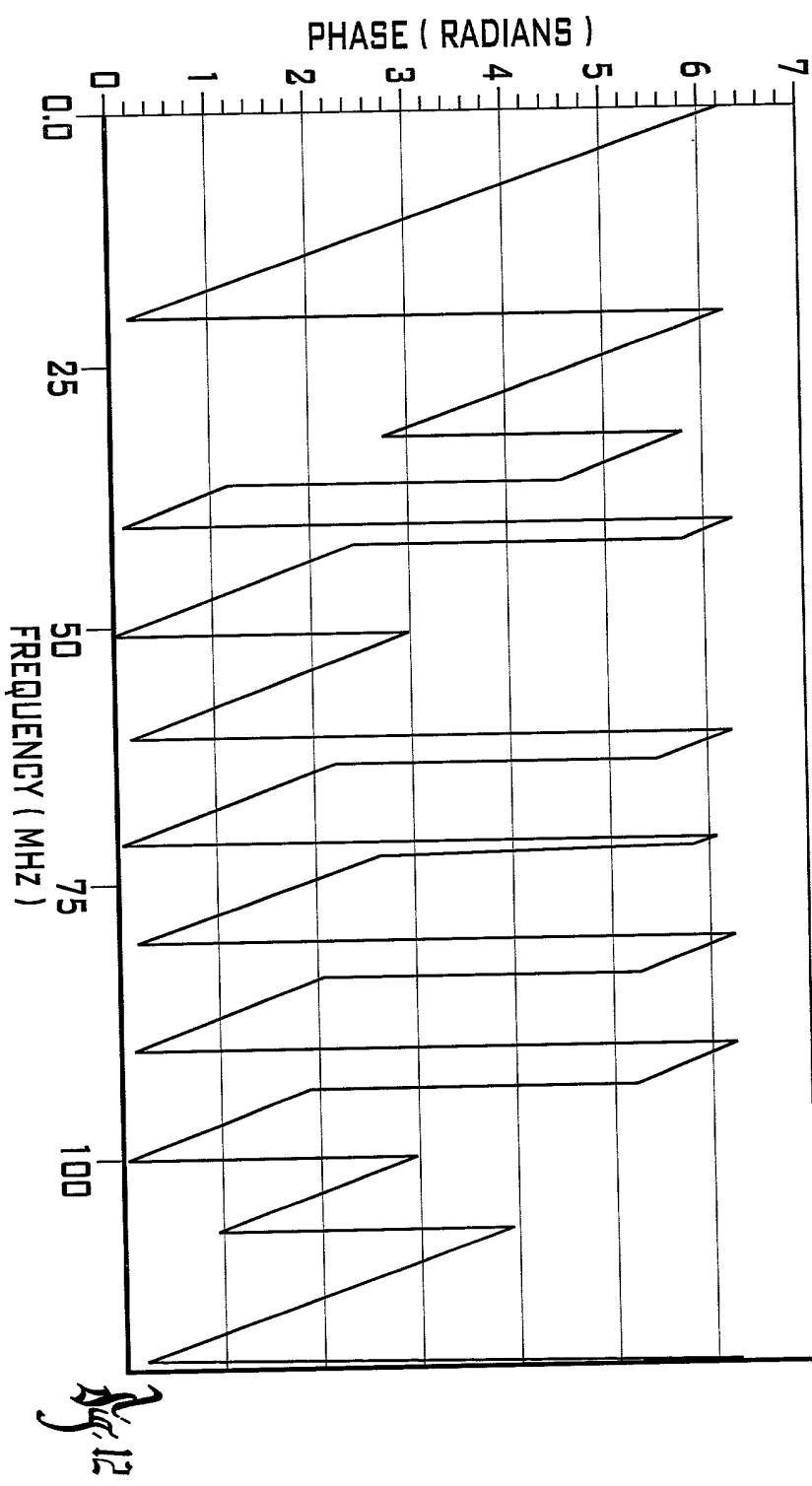


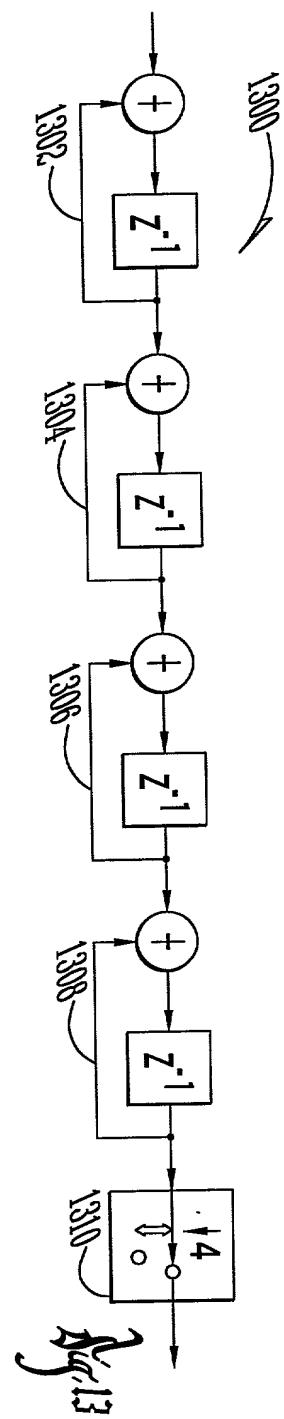


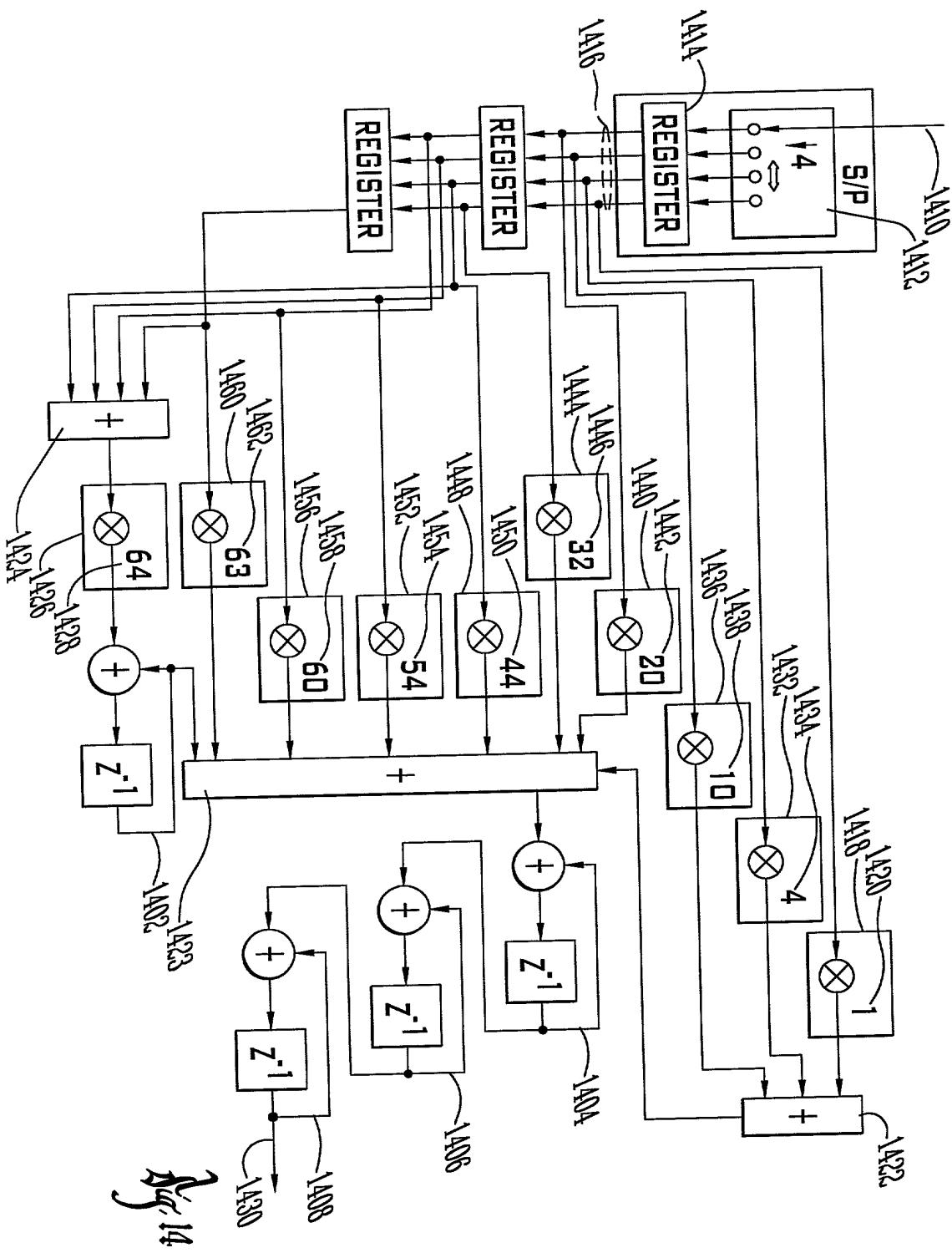




1102
1103







三

1 STAGES	0, A, A+B, A+B+C, A+B+C+D, A+B+C+D+E,...
2 STAGES	0, 0, A, 2A+B, 3A+2B+C, 4A+3B+2C+D, 5A+4B+3C+2D+E,...
3 STAGES	0, 0, 0, A, 3A+B, 6A+3B+C, 10A+6B+3C+D, 15A+10B+6C+3D+E,...
4 STAGES	0, 0, 0, 0, A, 4A+B, 10A+4B+C, 20A+10B+4C+D, 35A+20B+10C+4D+E,...
5 STAGES	0, 0, 0, 0, 0, A, 5A+B, 15A+5B+C, 35A+15B+5C+D, 70A+35B+15C+5D+E,...
6 STAGES	0, 0, 0, 0, 0, 0, A, 6A+B, 21A+6B+C, 56A+21B+6C+D, 126A+56B+21C+6D+E,...
7 STAGES	0, 0, 0, 0, 0, 0, 0, A, 7A+B, 28A+7B+C, 84A+28B+7C+D, 210A+84B+28C+7D+E,...
8 STAGES	0, 0, 0, 0, 0, 0, 0, 0, A, 8A+B, 36A+8B+C, 120A+36B+8C+D, 330A+120B+36C+8D+E,...

1500
1508
1504

STAGE N, OUTPUT M



+

STAGE N+1, OUTPUT M



Fig. 15

STAGE N+1, OUTPUT M+1

Fig. 16

1 STAGES	0, 1, 1, 1, 1, ...
2 STAGES	0, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, ...
3 STAGES	0, 0, 0, 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, 105, 120, 136, 153, 171, 190, 210, 231, 253, 276, 300, 325, 351, 378, 406, 435, 465, 496, 528, 561, 595, 630, 666, 703, 741, 780, 820, 861, 903, 946, 990, 1035, 1081, 1128, 1176, 1225, 1275, 1326, 1378, 1431, ...
4 STAGES	0, 0, 0, 0, 1, 4, 10, 20, 35, 56, 84, 120, 165, 220, 286, 364, 455, 560, 680, 816, 969, 1140, 1330, 1540, 1771, 2024, 2300, 2600, 2925, 3276, 3654, 4060, 4495, 4960, 5456, 5984, 6540, 7140, 7770, 8436, 9139, 9880, 10660, 11480, 12341, 13244, 14190, 15180, 16215, 17296, 18424, 19600, 20825, 22100, 2346, 24804, ...
5 STAGES	0, 0, 0, 0, 0, 1, 5, 15, 35, 70, 126, 210, 330, 495, 715, 1001, 1365, 1820, 2380, 3060, 3876, 4845, 5985, 7315, 8855, 10626, 12650, 14950, 17550, 20475, 23751, 27405, 31465, 35960, 40920, 46376, 52360, 58905, 66045, 73815, 82251, 91390, 101270, 111930, 123410, 135751, 148995, 163185, 178365, 194580, 211876, 230300, 249900, 270775, 292825, 316251, ...
6 STAGES	0, 0, 0, 0, 0, 1, 6, 21, 56, 126, 252, 462, 792, 1287, 2002, 3003, 4368, 6188, 8568, 11628, 15504, 20349, 26334, 33649, 42504, 5330, 65780, 80750, 98280, 118755, 142506, 169911, 201376, 237336, 278266, 324632, 376992, 435897, 50942, 57575, 658008, 749398, 850668, 96298, 1086008, 1221759, 1370754, 1533939, 1712304, 1906884, 2118760, 2349060, 2598960, 2869685, 3162510, ...
7 STAGES	0, 0, 0, 0, 0, 0, 0, 1, 7, 28, 84, 210, 462, 924, 1716, 3003, 5005, 8008, 12376, 18564, 27132, 38760, 54264, 74613, 100947, 134596, 177100, 230230, 296010, 376740, 475020, 59375, 736281, 906192, 1107568, 1344904, 1623160, 1947792, 2324784, 2760681, 3162623, 3838380, 4496388, 5245786, 6096454, 7059052, 845060, 9366819, 10737573, 12271512, 13983816, 15890700, 18009460, 20358520, 22957480, 25827165, ...
8 STAGES	0, 0, 0, 0, 0, 0, 0, 1, 8, 36, 120, 330, 792, 1716, 3432, 6435, 11440, 19448, 31824, 50388, 77520, 116280, 170544, 245157, 346704, 480700, 657800, 888050, 1184040, 1560780, 2035800, 2629575, 3365856, 4272048, 5379616, 6724520, 8347680, 10295472, 12620256, 15380937, 18643560, 2248940, 26978328, 32224114, 38320568, 45379620, 53524680, 62891499, 73629072, 86900584, 99884400, 115775100, 135784560, 154143080, 17710560, ...

1700

17

<u>PATH 4:</u>	
STAGE 4	1, 35, 165, 455, 969, 1771, ...
STAGE 3	1, 34, 130, 290, 514, 802, ...
STAGE 2	1, 33, 96, 160, 224, 288, ...
STAGE 1	1, 32, 63, 64, 64, 64, ...

<u>PATH 3:</u>	
STAGE 4	4, 56, 220, 560, 1140, 2024, ...
STAGE 3	4, 52, 164, 340, 580, 884, ...
STAGE 2	4, 48, 112, 176, 240, 304, ...
STAGE 1	4, 44, 64, 64, 64, 64, ...

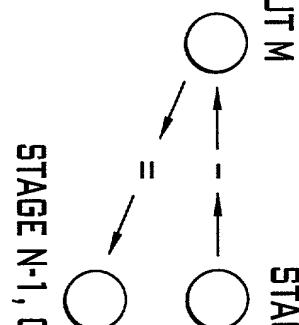
PATH 2:

<u>PATH 2:</u>	
STAGE 4	10, 84, 286, 680, 1330, 2300, ...
STAGE 3	10, 74, 202, 394, 650, 970, ...
STAGE 2	10, 64, 128, 192, 256, 320, ...
STAGE 1	10, 54, 64, 64, 64, 64, ...

PATH 1:

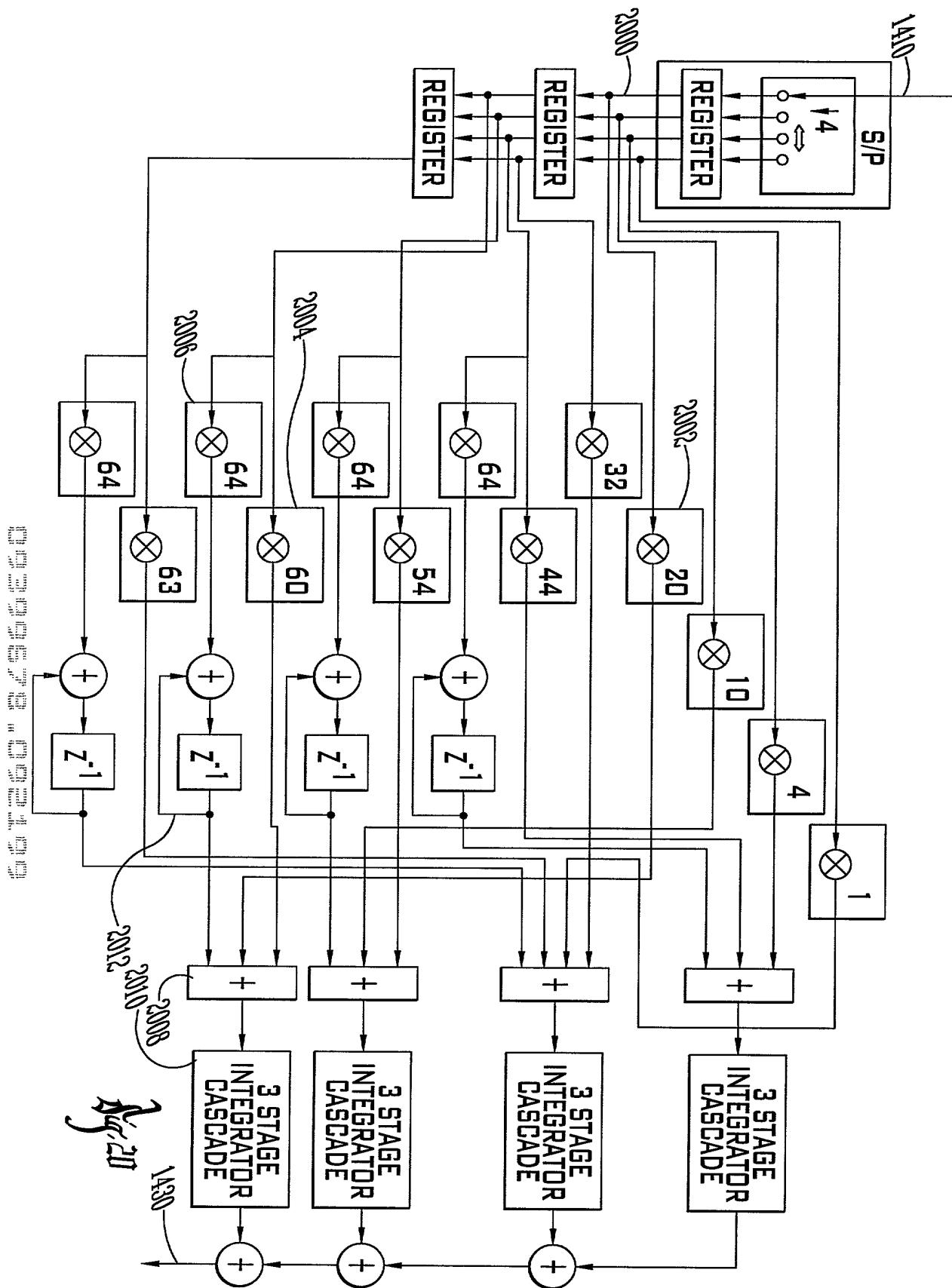
<u>PATH 1:</u>	
STAGE 4	20, 120, 364, 816, 1540, 2600, ...
STAGE 3	20, 100, 244, 452, 724, 1060, ...
STAGE 2	20, 80, 144, 208, 272, 336, ...
STAGE 1	20, 60, 64, 64, 64, 64, ...

STAGE N, OUTPUT M



STAGE N-1, OUTPUT M+1

14/19



$A, 4A+B, 10A+4B+C, \underline{20A+10B+4C+D}, 35A+20B+10C+4D+E, 56A+35B+20C+10D+4E+F, 84A+56B+35C+20D+10E+4F+G, \underline{120A+84B+56C+35D+20E+10F+4G+H}, 165A+120B+84C+56D+35E+20F+10G+4H+I, 220A+165B+120C+84D+56E+35F+20G+10H+4I+J, 286A+220B+165C+120D+84E+56F+35G+20H+10I+4J+K+L, 455A+364B+286C+220D+165E+120F+84G+56H+35I+20J+220C+165D+120E+84F+56G+35H+20I+10J+4K+L, 364A+286B+10K+4L+M, 560A+455B+364C+286D+220E+165F+120G+84H+56I+35J+20K+10L+4M+N, 680A+560B+455C+364D+286E+220F+165G+120H+84I+56J+35K+20L+10M+4N+O, 816A+680B+560C+455D+364E+286F+220G+165H+120I+84J+56K+35L+20M+10N+40P, \dots$

Fig. 21

PATH 1:

$\boxed{20A, 120A+20E, 364A+120E+20I, 816A+364E+120I+20M, \dots}$

PATH 2:

$\boxed{10B, 84B+10F, 286B+84F+10J, 680B+286F+84J+10N, \dots}$

PATH 3:

$\boxed{4C, 56C+4G, 220C+56C+4K, 560C+220C+56K+4O, \dots}$

PATH 4:

$\boxed{D, 35D+H, 165D+35H+L, 455D+165H+35L+P, \dots}$

PATH SUM:

$\boxed{20A+10B+4C+D, 120A+84B+56C+35D+20E+10F+4G+H, 364A+256B+220C+165D+120E+84F+56G+35H+20I+10J+4K+L, 816A+680B+560C+455D+364E+286F+220G+165H+120I+84J+56K+35L+20M+10N+40P, \dots}$

Fig. 22

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

Docket #98CR023/KE

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **Tailored Response Cascaded Integrator Comb Digital Filter And Methodology For Parallel Integrator Processing**, the specification of which

(check one) is attached hereto.

was filed on _____ as

Application Serial No. _____ and was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign applications(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) None

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

<u>Application Serial Number</u>	<u>(Filing Date)</u>	<u>(Status -patented, pending, abandoned)</u>
<u>Application Serial Number</u>	<u>(Filing Date)</u>	<u>(Status -patented, pending, abandoned)</u>

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Kyle Eppele, Reg. #34,155, James P. O'Shaughnessy, Reg. #27,667, John J. Horn, Reg. # 28,803, John M. Miller, Reg. # 38,560, Jay J. Deinken, Reg. # 28,406, and Walter R. Walbrun, Reg. # 37,464.

Address all telephone calls to Kyle Eppele at telephone no. (319) 295-8280

Address all communications to ROCKWELL COLLINS, INC.

Attention: Kyle Eppele M/S 124-323
400 Collins Rd. NE
Cedar Rapids, Iowa 52498

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor

Duane L. Abbey

Inventor's Signature

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Date 21 SEPT. 1999

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Cedar Rapids, IA 52402

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Date _____

Second Inventor's Signature

Citizenship _____

USA

Residence _____

Post Office Address _____

Full name of third joint inventor, if any

Date _____

Third Inventor's Signature

Citizenship _____

USA

Residence _____

Post Office Address _____